REL FOR ASM	QTY	TECHNICAL APPROVAL				DATE	EC NO.		DATE		PART NO. R3240-B0011-01	REV 01
		ELECTRICAL									DEVELOPMENT NO.	Q/M
		MATERIAL										

NOTES: Unless otherwise specified

1. General Requirement:
   a. Board shall be built per IPC-A-600 and IPC6012, class II, latest revision.
      Plating and annular rings must meet the Class 3 specification.
   b. Board shall be electrically tested per current revision of IPC 6012 and IPC 9252 class II.
      Completed electrical test Boards must be marked in permanent non-conductive ink.
      This identification stamp or Line must be in the same location on every board,
      and must not encroach onto any metallic surface, tooling holes, or fiducial clearances.
      PCB vendor shall ensure Etest marking traceability between quality conformance test
      circuitry and the manufacturing history.
   c. Configuration of the printed circuit board not specifically dimensioned on the
      drawing shall be controlled by the gerber data.
   d. Bow and Twist: shall not exceed .007" per inch.
   e. Fabrication Tolerances: end product trace widths and lands shall not vary more
      than the smaller of .001" or 20% of the trace width from the gerber data.
   f. PCB fabrication process and materials must be compliant with the Hazardous
      Substances (RoHS) Directive and compatible with Pb Free assembly process.
   g. Thieving is allowed all layers with 0.050" squares on 0.100" pitch and 0.100"min
      away from any designed features (i.e. vias, pads, traces, etc.).
   h. Unless specified otherwise, average copper thickness in plated through holes shall
      not be less than 0.001", with no single measurement less than 0.0008".
      measurement shall be taken per the IPC 6012 latest revision
   i. Non functional pads may be removed from internal layers.
   j. The entire assembly must be IEC/EN60950 compliant and be RoHS 6 compliant.

2. Via:
   a. Tangency is allowed on via size 8mil, 10 mils and 12 mils provided.
      Tear dropping is applied to the entry of the trace to the pad.

3. Drilling:
   a. All hole symbols may not be shown in the drawing. See Drill chart for details.
   b. Diameters in the drill table are finished hole sizes with +/-0.003" tolerance unless
      otherwise specified in the drill table.
   c. All press-fit hole size with +/-2mil tolerance

4. Marking:
   a. Soldermask,photo-imaged liquid polymer on both sides of boards in accordance
      with IPC-SM-840, Type B, Class 2, over bare copper. Soldermask color to be GREEN.
      matte finish materials preferred.
   b. Component Marking: Silkscreen both sides with white, non-conductive epoxy ink.
      Lands and exposed plated areas to be free of ink.
   c. Identification: PCB part number to be etched on component side.
      Fab vendor logo,UL marking(UL94V-0&UL file number),PWB UL type or model,
      date code to be placed on silkscreen solder side.

5. Backdrill legend:

   BOT SIDE: R3059-B0003-01_R01_bdl_14-4, Must not cut layer 3 (Stub length 7+/-5 mil tolerance)
             R3059-B0003-01_R01_bdl_14-6, Must not cut layer 5 (Stub length 7+/-5 mil tolerance)

   TOP SIDE: R3059-B0003-01_R01_bdl_1-9, Must not cut layer 10(Stub length 7+/-5 mil tolerance)
             R3059-B0003-01_R01_bdl_1-11,Must not cut layer 12 (Stub length 7+/-5 mil tolerance)

   **Note* Backdrill Legend is system generated from Cadence layout tool.
   The intergrity of connection to must not cut layers must be maintained.
   The vendor is requested to adjust backdrill plunge depths accordingly.
   Our NC drill documentation will include 2 backdrill files for bottom
   layer up plunges and 2 backdrill files for top layer down plunges.

6. Please provide drill bit size selected for all press-fit holes and average plating thickness
   in press-fit holes in DFM report.

7. All the dimensions in the drawing will statistically monitor the ongoing process quality control
   and require a minimal process control value of Cpk >=1.33. There are specified requirement about
   critical to function marked as CTF in the drawing, require a minimal process control value of Cpk >=1.67.

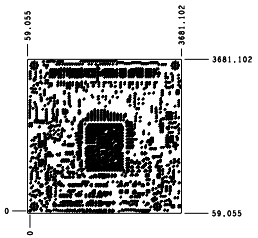
8. Please provide actual residual copper rate for each layer in DFM report.

9. Please provide actual hole measurement report for press-fit holes and non-PTH holes in a board.
   Send soft copy to GDS engineer, who release Gerber package. Hard copy is required in delivery report.

10. Please follow our stack-up in the gerber package.

11. For SI requirements,please refer the files in gerber package.

12. Please provide PCB working panel utilization in TQ report.



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
+	8.0	+0.0/-8.0	PLATED	1153
+	10.0	+0.0/-10.0	PLATED	1555
+	12.0	+0.0/-12.0	PLATED	32
⊞	106.0	+3.0/-3.0	PLATED	4
⌖	20.0	+2.0/-2.0	NON-PLATED	1
⌖	35.0	+2.0/-2.0	NON-PLATED	4
⌖	43.0	+2.0/-2.0	NON-PLATED	2
⌖	63.0	+2.0/-2.0	NON-PLATED	6

PART NO.	REV
R3240-B0011-01	01

MATERIAL NO.		MUST CONFORM TO ENG SPEC:		SCALE: 1:1	PART NO. R3240-B0011-01 REV 01
MAT'L ALTERNATE NO.		TOLERANCES UNLESS NOTED		THIRD ANGLE PROJECTION	TITLE DENVERTONCOME
		LINEAR ±	0.005"		FABRICATION DRAWING
CASE DEPTH		ANGLES ±	5 degree		DESIGNER Jane Zhao 2021/05/10
HARDNESS		RADII UNLESS NOTED			CHECKED Vivian Zhang 2021/05/10
SURFACE TREATMENT	CODE NO.	EDGE/CORNER BREAKS	OUTSIDE MAX		APPROVED Marco Qin 2021/05/10
			INSIDE MAX		CLASS

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